Exhibit 4

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Application of RF Circuit Design Principles to Distributed Power Converters

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Abstract—The application of RF circuit design principles to high-frequency power converters is described. Compared to conventional converter design, emphasis is placed on obtaining sinusoidal-type waveforms (instead of rectangular-type waveforms) to minimize device switching time requirements and alleviate transforming requirements. A 25-W 48-V to 5-V dc-to-cd converter design using a 5-MHz switching frequency is presented illustrating these principles, using a Class E power amplifier, an L section impedance transformer, and a shunt-mounted harmonically tuned rectifier circuit. Computer simulation results are presented that indicate the feasibility of the proposed design approach, specify required circuit parameters and indicate that line and load regulation can be achieved with narrow-band frequency control. Experimental results on a low power 5-W, 25-V to 5-V dc-to-dc converter breadboard using a 10-MHz switching frequency with the described circuit topology are presented. An efficiency of 68 percent was obtained and load regulation by frequency control demonstrated. Inductor Q requirements limit the conversion efficiency of the proposed converter, and will probably be the limiting factor in obtaining high efficiency with similar design approaches.

I. Introduction

RECENT trends indicate that typical methods of powering electronic equipments, in which large blocks of electronic circuitry are powered from a single source need to be reconsidered. The growing utilization of small, complex, building blocks of electronic circuitry is bringing about a need for space-conservation power conditioning modules. This powering alternative will provide design engineers with options to better balance power circuit design factors such as filtering, load regulation, overload protection, dc isolation, and EMI.

Module-based power conditioning will require higher quantity, lower power, smaller size power modules. These factors indicate that switching frequencies of dc-to-dc converters should be appreciably above the usual 20- to 50-kHz rate of conventional circuitry, and probably more than an order of magnitude higher than can be expected with classical switching circuits. High switching frequencies can lead to smaller circuit elements, particularly inductors and transformers, and smaller input and output filtering circuitry. Semiconductor devices are becoming available that allow the use of higher frequencies at the power levels being considered.

The purpose of this work was to investigate the applicability of RF circuit design principles to high-frequency power converters. This manuscript is organized in three main sections: first, a discussion of RF circuit design principles applicable to converters (Section II); second, the design of a 25-W, 48-V to 5-V 5-MHz converter (Section III), and evaluation of this design using computer simulation (Sections IV and V); third, preliminary experimental results on a 5-W, 25-V to 5-V 10-MHz converter using the same circuit topology (Section VI). Finally, the work is summarized (Section VII).

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II. RF Circuit Design Principles Applicable to Power Converter Design

As the switching frequency of power conditioning circuits is increased above approximately 1 MHz, conventional converter designs in which square pulses are generated with negligibly small switching times and rectified with Schottky diodes having negligible parasitics will become limited. Fortunately there are circuit approaches to switching inverters and rectifier circuits, key components in many converter implementations, which overcome these limitations. Some of these RF design concepts have been proposed for use in so-called resonant converters, but they will be briefly discussed as a group as listed below:

1) switching transistor waveform shaping to alleviate the requirements of switching times being short compared to the switching period;
2) generation of sinusoidal-type waveforms wherever possible rather than rectangular pulse waveforms;
3) incorporation of semiconductor device and passive element reactive parasitics into circuit design;
4) use of harmonic tank circuits to provide necessary harmonic currents and voltages for waveshaping.

Switching transistor waveform shaping is a key consideration in permitting high-frequency operation with a fixed device capability. It is the underlying principle in resonant converter design. The concept is simple: have the switching device change from "on" to "off" and "off" to "on" with negligible current flow through and voltage across the device respectively, thus minimizing switching loss without requiring the switching time to be a small fraction of the switching period. Unfortunately implementation is not straightforward and appreciably complicated (if not impossible) with rectangular waveforms.

Besides the limiting effect on switching device waveform shaping, rectangular pulses are undesirable at higher switching frequencies because of enhanced component requirements. For example, component loss is generally higher at the harmonic frequencies due to skin effect resistance in conductors

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and increased loss tangent in magnetic materials and some dielectrics. More important is the impedance transformation requirements, which in conventional converters must be broad band and usually involve magnetic transformers, while with sinusoidal waveforms inductor–capacitor L, T, and π sections can be used. Of course, harmonics must be generated near the switching and rectifying devices, but they should be localized and not "propagate" through the network.

The last two design factors listed above, parasitic elements and harmonic circuits, are not often used until VHF to UHF frequencies, but are probably useful above 1 MHz because of the power levels, load impedance levels, and efficiency requirements projected for many decentralized converters. Taking into account parasitic reactive elements in circuit design, rather than specifying small values, is not necessary at low frequencies but standard design procedure at higher RF frequencies. Examples of such parasitics include the nonlinear semiconductor junction capacitance, wiring and lead inductance, and parasitic coupling capacitances, even though proper circuit layouts are used. For proper design, these parasitics must be quantified using experimental characterization techniques.

Harmonic tank circuits can be a principal factor in waveform shaping while localizing harmonics. It is often used in RF parametric and mixing circuits and with highly nonlinear sources such as silicon trapped plasma avalanche transit time (TRAPATT) and gallium arsenide limited space charge accumulation (LSA) diodes. Although not necessary to achieve useful RF designs, this circuit technique should be considered by power converter designers if high switching frequencies, permitting easy realization of high Q resonant circuits (for example, using printed spiral inductors and chip capacitors or possibly even distributed resonators), are employed.

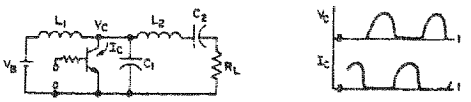
III. Design for 25-W, 48-V to 5-V Distributed Power Converter

In this investigation into high frequency dc-to-dc converters, a 25-W, 48-V to 5-V design objective was specified. The approach was taken as follows:

1) emphasize overall conversion efficiency as the key design goal, selecting RF circuit approaches most likely to achieve high efficiency;
2) use available RF designs, as much as possible, to realize the components of a dc-to-dc converter (sine wave inverter, single frequency transformer, rectifier with sine wave input);
3) load and line regulation and control circuit methodologies should be considered, but without expending effort in design implementations;
4) dc isolation would not be required, but the design should be amenable to including this feature if necessary;
5) input and output filtering requirements would not explicitly be considered, but the ripple amplitudes would be delineated.

Thus the key emphasis was to identify RF power circuit topologies with potentially high conversion efficiency, realizing that much additional design work is needed to obtain an operational power converter.

Fig. 1. RF circuit concept for dc-to-dc converters.



FIRST ORDER DESIGN EQUATIONS (WITH 50% DUTY CYCLE)

$$R_L = \frac{.5766 V_B^2}{P}$$

$$C_1 = \frac{.210}{\omega R_L}$$

$$\omega^2 L_2 C_2 = 1.35$$

$$\frac{\omega L_2}{R_L} = Q_L$$

$$\omega^2 L_1 C_1 = RR$$

DESIGN PARAMETERS SELECTED

$P = 25$ W $\quad Q_L = 5$

$V_B = 48$V $\quad RR = 10$

$f = 5$MHz OR $\omega = 3.142 \times 10^7$/sec

CIRCUIT PARAMETERS

$R_L = 53.16$ OHMS

$C_1 = 126$ pF

$L_2 = 8.5\ \mu$H

$C_2 = 162$ pF

$L_1 = 80.5\ \mu$H

Fig. 2. Basic Class E RF inverter design (after Sokal and Sokal [1], [3]).

The basic circuit approach selected consists of three constituents, a sine wave inverter, a single frequency impedance transformer, and a rectifier with sine wave input as depicted in Fig. 1. A Class E RF power amplifier was selected as the inverter, a capacitor–inductance L section as the impedance transformer, and a shunt-mounted harmonically tuned diode configuration as the rectifier. The design of each is discussed briefly below, followed by a discussion of the complete converter.

The basic Class E inverter using a bipolar switch as described [1] and patented [2] by the Sokals is shown in Fig. 2 along with first order design equations. Component values become fixed in this circuit after specifying the dc supply voltage (48 V), the power output (25 W), the switching frequency and the load external Q. A switching frequency of 5 MHz was selected, somewhat arbitrarily, as a frequency at which the circuit concepts can be easily implemented and components more easily characterized. Obviously this parameter affects component values and Q's and could significantly affect circuit realizability and cost. However, without a firm technology base, this important parameter could not be selected without exercising engineering judgement.

The load external Q involves the usual tradeoff between harmonic content in the load and parameter (L_2 and C_2) stress. This tradeoff is of greater concern in a converter requiring load regulation in that the Q decreases as the converter is more lightly loaded. A Q of 5 at full load was somewhat arbitrarily

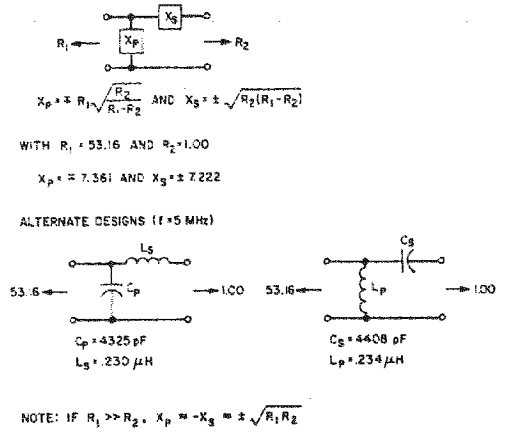


Fig. 3. Single frequency L section transformers (after Everitt and Anner [5]).

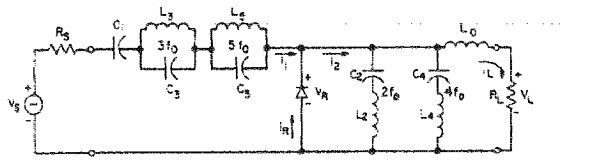


Fig. 4. Ideal shunt-mounted harmonically tuned rectifier (after Gutmann and Borrego [6]).

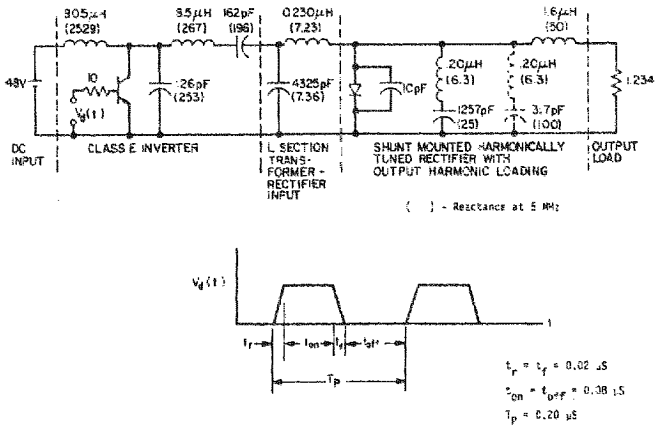


Fig. 5. Overall dc-to-dc converter.

selected. Using the equations of Fig. 2, the following parameter values were obtained: $R = 53.16\ \Omega$, $C_1 = 126$ pF, $C_2 = 162$ pF, $L_2 = 8.50\ \mu$H. Note that L_1 is an RF choke, whose reactance was chosen to be ten times the reactance of C_1 (i.e., reactance ratio $RR = 10$) resulting in a value of 80.5 μH. Additional articles by Sokal [3] and Raab [4] are recommended for more detailed design considerations and the effect of parameter tolerances in this design, respectively.

Since the Class E sine wave inverter (power amplifier) design results in a 53.16-Ω load resistance and the dc output is at a 1-Ω level full load (5 V at 5 A), a nominal 50:1 impedance transformer is needed prior to the rectifier stage (actual value required depends upon the rectifier circuit). A variety of L-C transformers are possible [5], but an L section was selected to minimize the number of components. Using a 53.16-Ω input impedance and a 1-Ω output impedance, the two designs depicted in Fig. 3 result. The C-L network was selected over the L-C network for an important reason: the C-L network provides harmonic isolation between inverter and rectifier, that is the C-L network is basically a low-pass filter while the L-C network is a high-pass filter.

Many low-frequency rectifier circuits are driven by ideal (i.e., zero impedance) voltage sources and in most conventional converters driven with rectangular pulses. In the Class E inverter C-L transformer circuitry, the rectifier will be driven from a sine wave generator with a finite equivalent resistive source impedance (at least under full load). While rectifier circuits developed at lower frequencies could be utilized, a high-frequency rectifier circuit originally described by Gutmann and Borrego [6] was selected because of a basic compatibility with the RF circuit design philosophy described earlier.

The ideal shunt-mounted harmonically tuned rectifier is shown in Fig. 4. The input resonators present an open circuit to the diode at the odd harmonics, while the input tuning capacitance provides a net zero input reactance at the fundamental. The output resonators present a short circuit at the even harmonics, and the output filter inductor a near infinite impedance at the fundamental and odd harmonics. Note that this circuit is more readily implemented at higher frequencies where the output resonators and inductance can be replaced by a quarter-wave length of nondispersive transmission line terminated in a large capacitance and the dc load. With lossless components, 100-percent conversion efficiency (dc output power divided by power available from ac generator) is obtained when the dc load resistance equals $\pi^2/8$ times the ac source resistance [6].

This circuit is not suitable for direct implementation due to the harmonic resonators required. However the C-L transformer can provide the suitable input impedance required as the inductive reactance of the transformer provides an adequately high impedance at the odd harmonics and the transformer capacitance provides isolation from the Class E inverter circuitry. Also, it was believed, as confirmed with computer simulation, that high efficiency could be maintained with a minimum number of output resonators. In fact, a single second harmonic resonator appears adequate, although including a fourth harmonic resonator could prove desirable (discussed in Section IV).

The output resonator and inductor parameter values were selected to give a reasonable loaded Q of about 10, and are not critical in the design. As the circuit is implemented, these values can be modified to simplify component realizability considerations, or perhaps be adjusted to aid in providing load and line regulation.

The resultant dc-to-dc converter using the Class E inverter, C-L transformer and modified shunt-mounted harmonically tuned circuit is shown in Fig. 5. The reference component values are shown, along with the fundamental frequency (5 MHz) reactance of the energy storage elements. Also shown is the base drive waveform assumed in the simulations. Note that the impedance transformer-rectifier interface is not well defined, as the transformer also provides the rectifier diode input impedance requirement (while isolating the inverter imped-

ance). However, the interface between the Class E inverter and the transformer remains well defined.

IV. Computer Simulation Results on 48- to 5-V 25-W Power Converter

In this section, computer simulation results obtained on the dc-to-dc converter design described in Section III are presented assuming nominal design conditions. Emphasis was placed on confirming the design approach described in Section III, evaluating "interface" considerations only considered qualitatively in the design approach described previously, particularly the *C-L* transformer as the rectifier input harmonic control circuitry, evaluating the effect of a minimum number of rectifier output even harmonic resonators, and specifying component values and stresses for circuit implementation.

In this work, the Spice circuit analysis program [7] was utilized. Generic type device models were used and, in most cases, reactive element *Q*'s were not explicitly modeled. While certainly a limitation in prediction of conversion efficiency, lack of available data prevented such a desirable simulation. As a result, the overall dc-to-dc converter design was not optimized after simulating the circuit shown in Fig. 5, as such an effort was not warranted without more exact device and circuit element *Q* values. However, additional effort was placed on evaluating load and line regulation performance of the converter (described in Section V) and evaluating inductor *Q* necessary for high efficiency.

The computer simulation results with the Class E inverter design depicted in Fig. 2 were similar to the characteristics described in the literature [1]-[3] and the *C-L* transformer behaved as designed. The peak voltage on the switching transistor is 3.7 times the supply voltage (178 V compared to 48 V) while the peak switch current is 2.8 times the average supply current (1.3 A compared to 0.465 A). Therefore, the $I_{max}V_{max}$ rating of the switching transistor must be ten times the input dc supply power. With presently available bipolars and MOSFET's, power handling is not a key limitation. However, the device cost is increased as the $I_{max}V_{max}$ rating is increased (larger chip area) and the increased output capacitance can be a concern in the circuit design. The limitation, i.e., switching device stress, will be a factor in all inverter designs using a single switching transistor, although the $I_{max}V_{max}$ rating magnification may be different than with the Class E inverter.

Computer simulations of the harmonically tuned rectifier focused on demonstration that the *C-L* input filter provided sufficiently high odd harmonic impedance and that high efficiency could be obtained with a minimum number of output resonators. In these simulations, a sinusoidal 5-MHz source with 96-V peak amplitude and 53.16-Ω source impedance was used to replace the Class E inverter. The power available from this generator is 21.7 W comparable to the 25-W goal and suitable for evaluation purposes. The voltage across the rectifier diode is not a square wave [6] as in the ideal harmonically tuned rectifier, while the current through the diode is more nearly the ideal output half sinusoid. Additional harmonic resonator circuits result in more ideal waveforms. However, even with a single ($2f_0$) output resonator, conversion efficiency remains high. For example, with one output resonator, the output voltage is 4.55 V, increasing to only 4.65 V with four resonators.

TABLE I
Stress Levels on Components in 25-W 48-V to 5-V dc-to-dc Converter

Devices	
Switching Transistor	185V peak 1.8A peak
Rectifying Diode	15V reverse peak 16A forward peak
Capacitors	
C_1 = 126 pF	185V peak
C_2 = 162 pF	50V dc plus 230V ac*
C_{tr} = 4325 pF	5V dc plus 55V ac*
C_{2f_o} = 469 pF	5V dc plus 50V ac†
Inductors	
L_1 = 80.5 μH	.68A dc with .035A amplitude ripple
L_2 = 8.5 μH	1.2A ac*
L_{tr} = .23 μH	7.8A ac*
L_{2f_o} = .54 μH	3.1A ac†
L_f = 1.6 μH	4.7A dc plus 0.2A ripple

* 5 MHz ac frequency

† 10 MHz ac frequency

Note: All ac amplitudes are peak values.

TABLE II
Inductor Loss Considerations in 25-W 48-V to 5-V dc-to-dc Converter

Symbol	Inductor Valve (μH)	Resistance for 1W Dissipation (ohm)		Effective Q
L_1	80.5	2.2	(DC)	--
L_2	8.5	1.4	(5 MHz)	190.
L_{tr}	.23	.033	(5 MHz)	220.
L_{2f_o}	.54	.21	(10 MHz)	160.
L_f	1.6	.045	(DC)	--

When the overall converter shown in Fig. 5 was simulated, the switching transistor and rectifier diode waveforms were similar to those for individual components of the converter, confirming the design approach described in Section III. Similarly, the waveforms obtained for the load voltage, input current, Class E inverter output and transformer capacitance current are as expected. The overall efficiency was 85 percent with 5.84-V and 27.6-W dc output. The power dissipated occurs in the assumed 1-V recitfier diode drop, a high value being assumed to partially compensate for neglecting circuit loss. The power dissipated in the switching transistor is negligible.

Component stresses with this converter design are given in Table I. Of particular note is the voltage across the switching transistor, forward current through the rectifying diode, and current levels through inductors L_{tr}, L_{2f_o}, and L_f. While the semiconductor devices required are either commercially available or appear to be within the state of the art, the inductor requirements are formidable. Allowing 1 W of dissipation per inductor (a reasonable requirement), effective *Q*'s of about 200 are needed, as shown in Table II. It is clear that inductor

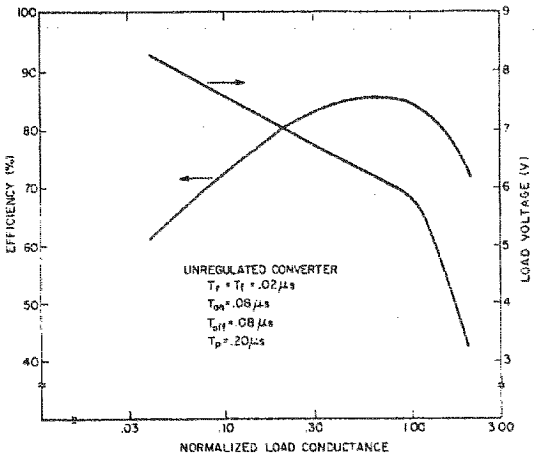


Fig. 6. Unregulated converter efficiency and load voltage with static load variations.

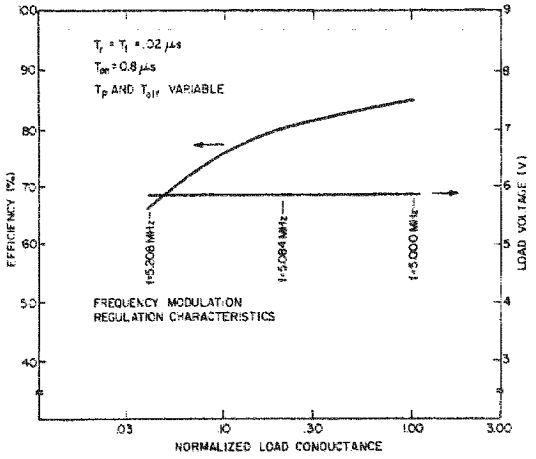


Fig. 7. Frequency regulated converter efficiency and load voltage with static load variations.

loss could be a serious obstacle to the implementation of the proposed converter, and further design work should attempt to minimize inductor Q requirements.

V. Load and Line Regulation Characteristics of Proposed Converter

In this section, computer simulation results on the regulation characteristics of the proposed dc-to-dc converter are presented. The design presented in Section III and with full load characteristics described in Section IV will be assumed throughout. Emphasis was placed on methods amenable to electronic control, that is, pulsewidth control (PWC) and frequency control (FC), rather than controlling circuit element values. Emphasis was placed on providing load regulation, which is more difficult to characterize than line regulation. To first order $V_{out} \propto V_{batt}$ in this design, so any technique that can provide load regulation was expected to be easily applicable to line regulation.

The proposed converter does not approximate an ideal (zero impedance) voltage source, and therefore the performance as the load is varied does not resemble conventional converters. The inherent unregulated converter characteristics are shown in Fig. 6, in which efficiency and load voltage are plotted as a function of normalized load conductance. The normalized load conductance is unity at the designed load of 1.234 Ω (efficiency is 85 percent and load voltage is 5.84 V as presented in Section IV). The normalized load conductance is varied from 0.04 to 2.00, that is, from $\frac{1}{25}$ to twice full load. The drive pulse characteristics, originally presented in Fig. 5, are shown for later comparison.

The efficiency peaks at the nominal designed load value, as expected in an impedance matched RF design, and remains relatively high from 10- to 200-percent load (efficiency above 72 percent). However, the voltage decreases rapidly with increasing load, a characteristic which must be corrected in most converter applications. The regulation results with PWC and FC will be discussed at 20-percent load, similar trends being observed at other loads.

As the on-time is reduced below 0.08 μs in PWC, characteristics remain relatively constant from 0.08 to 0.03 μs, but change rapidly below 0.03 μs. The load voltage equals the full load value of 5.84 V at an on-time of approximately 0.019 μs. Unfortunately, the efficiency drops to approximately 59 percent, the increased loss principally due to dissipation in the switching transistor. The performance is actually comparable to that of a linear regulator, and the sensitivity of output voltage to on-time indicates that the on-time control required would not be easily achieved.

As the period is varied by means of FC, the conversion efficiency is relatively unchanged while the load voltage is a strong function of frequency. With $T_p = 0.1967$ μs (frequency = 5.084 MHz) the load voltage is the desired 5.8 V. The performance (efficiency remaining high as the load conductance is reduced) is vastly improved compared to either PWC or a linear regulator. Also, FC could be more easily implemented with a voltage-controlled oscillator (VCO) in the driver stage.

The predicted performance of the frequency modulated converter is shown in Fig. 7. There is little change in the efficiency between the frequency regulated characteristic and the inherent converter efficiency dependence upon load shown in Fig. 6. However, the constant load voltage dependence upon normalized load conductance (equal to normalized load current) is much more desirable. It should be noted that the efficiency calculation at very light loads (normalized load conductance of 0.04) is only approximate as the simulation requires a long time to reach steady state.

With frequency control to obtain load regulation, there are some changes in device waveforms worth noting. First, the peak switching transistor voltage and peak diode voltage are somewhat higher (20 and 30 percent, respectively) while the current waveforms are significantly different. The rectifier diode current is reduced by a factor of nearly 5, while maintaining the same shape. However, the switching transistor has approximately the same peak current, but the average current is reduced due to a large negative current (in practice handled by a collector-to-emitter diode). Second, the load ripple is appreciably increased by a factor of almost 4 (expected for the inductive output filter), and the input current amplitude variation is unchanged as expected. Third, the voltage waveshape at the Class E inverter load is appreciably nonsinusoidal

TABLE III
COMPARISON OF NONREGULATED AND FREQUENCY REGULATED CONVERTER AT 20-PERCENT LOAD WITH FULL LOAD CONVERTER

	FULL LOAD	20% LOAD	
		NONREGULATED	FREQUENCY REGULATED
Frequency(MHz)	5.000	5.000	5.085
Load Resistance(ohms)	1.234	6.170	6.170
Load Voltage(V)	5.84	7.05	5.84
Efficiency(%)	85.	80.	83.
Peak Switch Voltage(V)	181.	205.	208.
Peak Switch Current(A)	1.8(and-0.1)	1.5(and -0.7)	1.3(and -0.8)
Peak Rectifier Voltage(V)	15.1	6.1	6.1
Peak Rectifier Current(A)	16.0	4.1	3.3
Input Current(A)	.675	.21	.145
RF Voltage Class E(V)	61.0	17.0	18.0
Load Ripple(p to p)(V)	.50	2.7	2.1
Input Current Ripple(p to p)(A)	.07	.08	.07
Harmonic Tank Circuit Current(p)(A)	2.9	1.4	1.1

as the inverter load external Q is near unity. Many of these waveform changes are similar for the unregulated converter but the differences will not be discussed. Many of these factors are quantified in Table III.

With light load, the load voltage is expected to increase due to both the rectifier [6] and the Class E inverter [4]. In fact, a more rapid rise in voltage with decreasing load would be anticipated by considering these components individually. The rise in voltage is partially alleviated by the L section transformer as the increase in input impedance of the rectifier at light loads is inverted in the impedance transformer, tending to increase the load on the inverter. This is observed by the reduced voltage across the Class E inverter load. In fact, it may be feasible to design a multistage impedance transformer that results in inherent load regulation, at least over a restricted range of load conductance.

The principal effect of the slight frequency change is thought to be the rectifier harmonic tank circuit impedance. As this circuit is detuned, less second harmonic current flows in the diode and the circuit is more lightly loaded. Although the reduction in second-harmonic current is only 30 percent as shown in Table III, it is felt that this reduction is a key contributor to the narrow-band frequency control load regulation. The load regulation frequency dependence is expected to be controllable by varying the Q of this tank circuit. However, this must be verified in further work.

VI. Preliminary Experimental Results on a 5-W 25-V to 5-V Breadboard Converter

A breadboard converter was designed, constructed, and evaluated in order to verify the computer simulation results and demonstrate the feasibility of the circuit topology described previously. Emphasis was placed on demonstration of power train efficiency and FC load regulation. To reduce laboratory development time, a commercially available Class E RF power amplifier demonstration unit[1] was used as the inverter. The capabilities of this unit [7] fixed the design parameters for the remainder of the converter.

The switching transistor and Schottky rectifier diode were somewhat arbitrarily selected. The Class E power amplifier is tuned with a RF bipolar switching transistor and in the unit utilized in this work an RCA Model 2N3262 was installed and used throughout. A Motorola silicon Schottky Model 1N5822 was selected from a group of readily available devices because it could handle the calculated voltage and current stress with minimum depletion layer capacitance (300 pF at 3 V decreasing to 85 pF at 30 V).

The transformer–rectifier circuitry was assembled on Teflon fiberglass board using ground plane construction. Air core inductors were wound using enamel-coated 16 gauge (52-mils diameter) copper wire on an approximately $\frac{5}{8}$-in diameter form (the larger filter inductor was wound on a 1-in diameter core). Ceramic NPO capacitors were used in the transformer and harmonic tank circuit, with a 20-pF air trimmer capacitor added in parallel for ease in tank circuit turning.

The dc-to-dc circuit was tested after tuning the RF amplifier into a 50-Ω load. Initially the inductors in the transformer and tank circuit and the trimmer capacitor were adjusted, and the dc load resistance was varied. A dc-to-dc power train conversion efficiency of 62 percent was obtained. Then the Class E inverter was adjusted to optimize compatibility with the transformer-rectifier unit. A power train conversion efficiency of 68 percent resulted with a 4.25-W power output and a 22-V to 4.25-V conversion. The optimum load resistance was 4.2 Ω and the switching frequency (f_o) was 10.141 MHz.

Considering that there was no iteration on the design, these results are considered very promising in verifying the potential of high-frequency dc-to-dc converters and in confirming the design technique described in Section III. While detailed measurements were not performed, the loss is attributed approximately as shown in Table IV.

Key waveforms for the 22-V to 4.25-V, 4.25-W converter at full load are depicted in Fig. 8. The switching transistor voltage is as predicted with the simulation, peaking at 84 V (3.82 V_B), while the rectifier diode has a low reverse plateau of 3 V prior to the peak of 23 V rather than an additional peak as in the simulation. This is attributed to the smoothing effect of the Schottky diode depletion layer capacitance in the experimental unit. The inverter output voltage is nearly sinusoidal with a dc level equal to the output voltage, similar to the computer simulation, while the output voltage shows the ripple predicted with the inductive output filter. This ripple

[1] Model E10-3, available from Design Automation, Lexington, MA.

TABLE IV
ESTIMATED LOSS CONTRIBUTIONS IN BREADBOARD CONVERTER

	Estimated Loss in Efficiency (%)
Switching Transistor	2%
Schottky Rectifier	10%
Output Inductor in Inverter (L_2)	3%
Transformer Inductor (L_{tr})	5%*
Tank Circuit Inductor (L_{2fo})	5%*
Input Inductor (L_1)	2%
Output Filter Inductor (L_f)	2%
Capacitors	2%
Wiring Loss	1%
TOTAL	34%

* Q of 125 at 10 MHz, increasing to 190 at 20 MHz as measured on Boonton Type 260A Q meter.

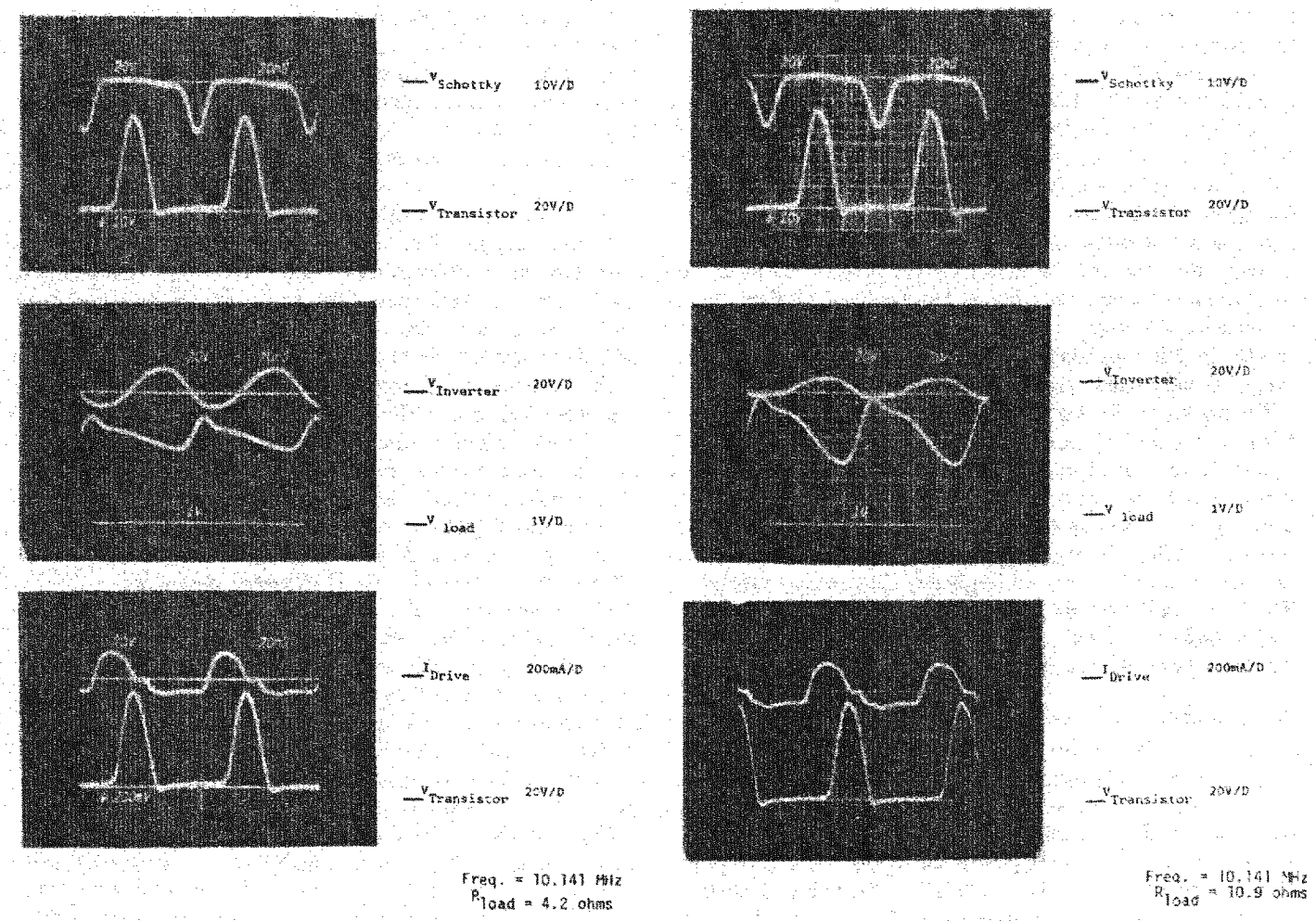


Fig. 8. Waveforms of breadboard converter at full load (R_{load} = 4.2 Ω and frequency = 10.141 MHz).

Fig. 9. Lightly loaded, unregulated converter waveforms (normalized load conductance = 0.39 and frequency = 10.141 MHz).

can be partially removed with a capacitance added in parallel with the load, a 0.068-μF capacitance reducing the peak to peak ripple to 0.2V.[2] The drive current to the base of the bipolar is also shown in Fig. 8, and indicates that the Class E switching waveform is not seriously affected by the efficiency optimization tuning described earlier.

Various measurements were taken with increased load resistances (lighter loading) and variable frequency to evaluate FC load regulation. Typical results are shown in Figs. 9 and 10 and Table V with 10.9-Ω load (normalized load conductance of 4.2/10.9 or 0.39) for the optimum full load frequency

[2] Additional filtering to reduce the ripple to the millivolt level required in many applications can be accomplished with classical techniques.

TABLE V
COMPARISON OF FULL LOAD AND REGULATED AND UNREGULATED BREADBOARD CONVERTER AT 39-PERCENT LOAD

	FULL LOAD	0.39 NORMALIZED LOAD CONDUCTANCE FREQUENCY UNCHANGED	0.39 NORMALIZED LOAD CONDUCTANCE FREQUENCY REGULATED
Load Resistance(ohms)	4.2	10.9	10.9
Frequency(MHz)	10.141	10.141	10.646
Load Voltage(V)	4.24	4.58	4.24
Load Voltage Ripple(p to p)(V)	1.5	3.0	2.5
Input Current(A)	.282	.158	.116
Efficiency(%)	68.	55.	65.
Inverter Output(p to p)(V)	27.	19.	21.
Peak Switching Transistor Voltage(V)	84.	85.	80.
Peak Rectifier Voltage(V)	23.	23.	19.

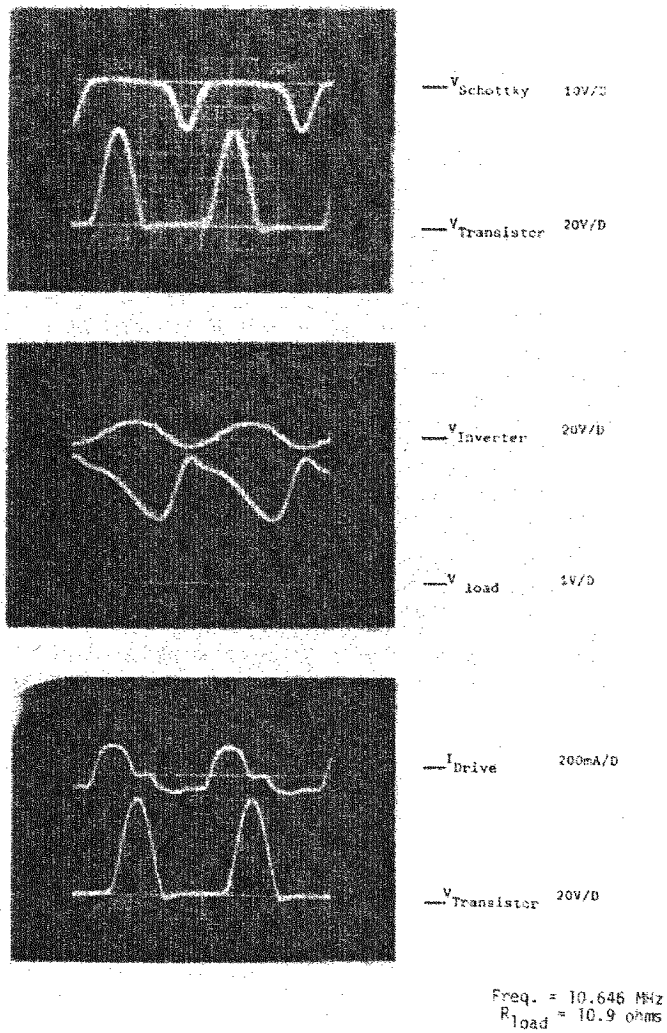


Fig. 10 Lightly loaded, frequency regulated converter waveforms (normalized load and conductance = 0.39 and frequency = 10.646 MHz).

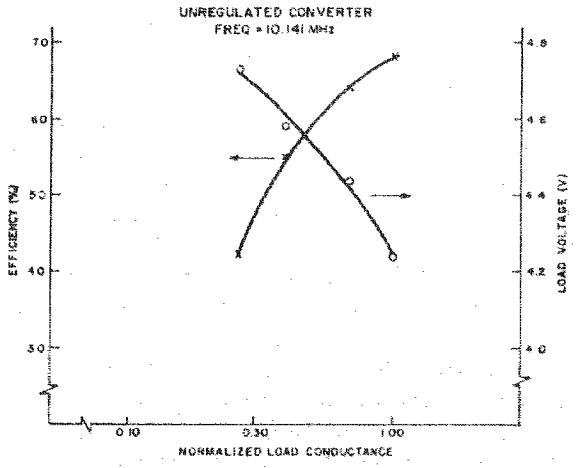


Fig. 11. Efficiency and load voltage as a function of load for unregulated breadboard converter.

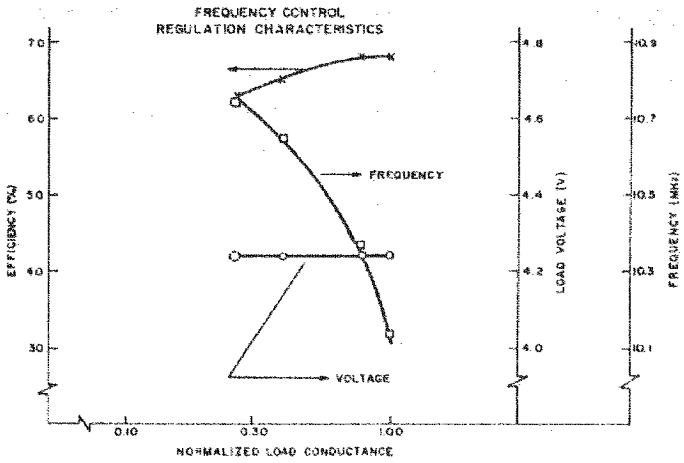


Fig. 12. Efficiency and load voltage as a function of load for frequency regulated breadboard converter.

(10.141 MHz) and load voltage regulated frequency (10.646 MHz), respectively.

When the load resistance was initially increased (Fig. 9), the voltage across the switching transistor (originally 84 V) increased and was limited to 85 V by a Zener diode in the Class E amplifier, thus protecting the RF transistor. The resulting distortion affects the efficiency and limits the increase in output voltage. Note that the RF voltage across the inverter output drops appreciably and the ripple in the output increases as predicted in the computer simulation. The switching losses are increased, as indicated by the overlap between base drive current and collector voltage.

When the frequency is increased to provide load regulation, the input dc current is reduced and the efficiency rises from 55 to 65 percent, near the full load value of 68 percent. Besides the reduction in output voltage (4.24 V instead of 4.58 V), the load voltage ripple decreases and inverter output RF voltage increases as predicted in the computer simulation. Note that the device voltage stresses are now below the full load values, unlike the computer simulation results. However,

the effect of the Zener protection diode on the nonregulated, lightly loaded converter and the difference in design specifications prevent an exact comparison with simulation results.

Using different loads, the data presented in Figs. 11 and 12 shows the efficiency and load voltage as a function of load for the unregulated converter and frequency regulated converter, respectively. As mentioned, the Zener diode across the Class E switching transistor affects the unregulated converter characteristics, resulting in a sharper falloff in efficiency and a more gradual rise in voltage with decreasing load. The performance obtained with FC is impressive and demonstrates that high-frequency designs can indeed be load (and line) regulated with little sacrifice in efficiency.

VII. Summary

RF design principles were applied to the design of high frequency (5 to 10 MHz) dc-to-dc power converters. A circuit topology consisting of a Class E inverter, *C-L* impedance transformer and shunt-mounted, harmonically tuned rectifier was chosen with advantages and disadvantages described in detail. Computer simulation results on the 5 MHz, 25 W, 48 V to 5 V converter verified the basic design approach and indicated that efficient load and line regulation could be provided with narrow-band frequency control.

A breadboard 10-MHz 5-W 25-V to 5-V converter was designed, constructed and evaluated using an RF bipolar switch and Schottky rectifier. In the first implementation, 68-percent power stage conversion efficiency was obtained, and the load regulation capability using FC was demonstrated. It is estimated that 75-percent efficiency could be obtained with component refinement, particularly optimization of inductor Q.

The key limitation on efficiency in the proposed design is attributed to inductor Q. Switching losses in the switching device, rectifier losses, and voltage and current stresses are sufficiently low that semiconductor device capability is not presently limiting. Further design work on high-frequency power converters utilizing the RF design concepts outlined in Section II should specify inductor Q as a design constraint.

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